SERIAL NO. 09/384692

PATENT
Docket RAL919990080US1

CERTIFICATE OF MAILING (37 C.F.R. 1.8(a))
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by Karen Orzechowski Signature: Karen Orzechowski

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

In re application of B. M. Bass, et al.	:	Date: July 20, 2004 IBM Corporation - IP Law 9CCA/B002
	:	P.O. Box 12195
Serial No. 09/384,692	:	Research Triangle Park,
	:	North Carolina 27709
Filed: 8/27/1999	:	Customer Number 25299
	:	
For: NETWORK SWITCH AND COMPONENTS AND METHOD OF OPERATION	:	Unit: 2155
	:	
	:	Examiner: Khanh Q. Dinh

APPEAL BRIEF

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the Final rejection of claims 10-13, 43 and 44 of this application. An appendix containing a copy of the claims is attached.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation (IBM), Assignee of the present application.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

Claims 1-42 were presented for examination. The Examiner issued restriction requirements partitioning the claims to inventions as follows:

(a) Claims 1-9

(a1) Claims 10-13 were originally grouped with (a) but the Examiner changed his mind and further partitioned the claims into (a) and (a1)

(b) Claims 14-25

(c) Claims 26-32 and 37

(d) Claims 33-36 and 38-42

Appellants elected claims 10-13 for examination. The non-elected claims were canceled without prejudice and will be prosecuted in subsequent applications. Claims 43 and 44 were added by amendment. Claims 10-13, 43 and 44 are in this appeal.

IV. STATUS OF AMENDMENT

No amendment has been filed subsequent to the Final Rejection.

V. STATEMENT OF INVENTION

The invention relates to a method of handling data flow through an interface device or network processor (the terms are used interchangeably, page 6, lines 9-10). The handling may include frame or packet classification, modification routing or like activities. The network processor is packaged in a switch router or like devices.

Figure 1 shows a block diagram of the network processor including a substrate 10 on which a plurality of subassemblies are integrated on said substrate (pages 11 through 13). In all such structures silicon real estate is at a premium and any technique or method reducing the components needed to accomplish a task is an improvement to this technology.

The sub-assembly of interest is the Embedded Processor Complex (EPC) 12, details of which are shown in Figure 12A. The EPC includes a plurality of picoprocessors N coupled to a single instruction memory in which picocode for forwarding frames or packets is stored and is used by all N processors. A general purpose processor such as a PowerPC is provided on the chip or external and communicates with the EPC. The location of the general purpose processor is identified as the Control Point. (Page 20, lines 16-23 and page 21, line 1; page 21, lines 19-23 and page 38, lines 23 through page 39, lines 1-6).

VI. ISSUES

Whether claims 10-13, 43 and 44 are unpatentable under 35 USC 102(b) as being anticipated by Shobatake et al. (U.S. Patent No. 5,557,609).

VII. GROUPING OF CLAIMS

There is only one group consisting of claims 10-13, 43 and 44. The claims of the single group do not stand or fall together.

VIII ARGUMENTS

A1. SHOBATAKE ET AL. DOES NOT TEACH ELEMENTS OF CLAIMED INVENTION

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. Vordegaal Bros. V. Union Oil Co. of California, 814 F. 2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987).

Shobatake et al. Figure 1 teaches a plurality of interface processors 102-1 through 102-N coupling individual ports 101-1 through 101-n of a switching system to the switch 103. As set forth at column 4, lines 40-56, each of the interface processors has a main memory only one of which is shown and number 11023 in Fig. 1. As stated in column 4, lines 52-55, "The processor 11021 includes an ALU and a sequencer used for channel-processing in the present invention, and further a channel processing

procedure code executed by the processor 11021 is written in the main memory 11023." Because the reference clearly teaches that each of the interface processors 1002-2 through 102-N are structured as the one shown in 102-1 it is clear that each of these processors has its own main memory from which it executes instructions as set forth at column 4, lines 52-55. Therefore, contrary to the Examiner's position (discussed hereinafter) the reference does not show or teach

> storing in a single instruction memory instructions for handling of data transiting an interface device;
>
> executing in a plurality of interface processors the instructions stored in the instruction memory;

Because neither of these elements are found expressly or inherently in Shobatake et al. the claims are not anticipated and are, therefore, patentable.

A2. Patentability of Claim 11

Claim 11 –due to its dependency on Claim 10– is patentable over Shobatake et al. The argument set forth above is equally applicable and is incorporated herein by reference.

In addition, Claim 11 is separately patentable in that it calls for " . . . storing selected portions of the parsed data flow in data memory, and directing other selected portions of the parsed data flow to a switching fabric for determination of an outbound direction".

No such process is practiced in Shobatake et al. Instead, Shobatake et a. partitioned a data stream into ATM cells and forwards all the cells through cell switch 103, Figure 1, col. 5, lines 41-65. Because Shobatake does not teach (expressly or

inherently) storing selected portion of the parsed data flow in data memory and directing other selected portion of the parsed data flow to a switching fabric claim 11 is not anticipated.

A3. Patentability of Claim 12

Claim 12 –due to its dependency on claims 10 and 11, respectively– is patentable over the art of record for reasons set forth above and incorporated herein by reference.

In addition, claim 12 is separately patentable. It calls for recombing stored and other selected portions of data flow prior to direction of the data flow outbound through an output port. Claim 12 depends on claim 11. So the recombination involved the selected portion of data flow stored in data memory with selected portions of the data flow directed to the switching fabric. In contrast Shobatake directs all portions of a data flow through cell switch 103, Figure 2. None is stored and then recombined as recited in claim 12. As a consequence claim 12 is not anticipated by Shobatake et al.

A4. Patentability of Claim 13

Claim 13, due to its dependency on claim 10, is patentable over Shobatake et al. The argument set forth above is equally applicable and incorporated herein by reference.

In addition, claim 13 is separately patentable in that it calls for parsing data flow into portions and distributing the parsed portions among the plurality of interface

processors for handling in parallel.

In Shobatake et al. each interface processor 102-1 through 102-n (Figure 1) and its associated interface point accommodation circuits 101-1 through 101-n operate as independent unit. Any data flow presented to an interface processor is partitioned into cells which are presented to the cell switch but not distributed among the interface processors for handling in parallel as recited in claim 13. As a consequence the claim is not anticipated and is patentable over the art of record.

A5. Patentability of Claim 43

Claim 43, due to dependency on claim 10, is patentable over Shobatake et al. The argument supporting patentability of claim 10 is equally applicable and incorporated herein by reference.

In addition, claim 43 is separately patentable in that it calls for "storing in control processor control information including initialization and configuration data; and

forwarding stored information to selected ones of said plurality of interface processors" which is not present in Shobatake et al. Instead, Figure 4 of Shobatake et al. shows a plurality of independently controlled interface processors 102-1 to 102-n. There is no control processor in which initialization and configuration data is stored and forwarding of the store information to selected one of said plurality of interface processors.

Because the elements of claim 43 are not present (explicitly or inherent) in Shobatake et al. the claim is not anticipated. See Vordegaal Bros. V. Union Oil Company of California (oppo. cited).

Claim 44 stands or falls with claim 43 and/or claim 10.

B. RESPONSE TO EXAMINER'S CONTENTION

With respect to appellants' argument made in the amendment dated October 13, 2003 to support patentability of claims 10-13, 43 and 44, the Examiner in the final rejection (paper #15) states: (a) "Applicants' arguments with respect to claims 10-13, 43 and 44 have been considered (underlining being that of appellants) but are moot in view of the new ground(s) of rejection" Final Office Action, page 4, item 4.

It appears as if the Examiner erred in this regard in that the rejection made in the Final Office Action, mailed 12/01/2003, paper #15, is the same rejection made in a previous Office Action mailed 7/16/2003, paper #13. In both Office Actions claims were rejected under 35 USC 102(b) as being anticipated by Shobatake et al.

Furthermore, it appears as if the Examiner erred in concluding elements of appellants' claimed invention are found in the reference. Such conclusion is necessary to make out a rejection based upon anticipation.

With respect to claim 10, the Examiner identified portions of Shobatake et al. which meets the first (storing . . .) and second (executing . . .) acts of appellants' claimed invention.

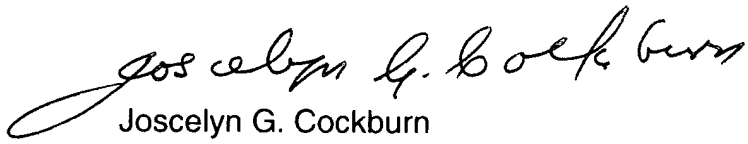
A review of Shobatake et al. including sections identified by the Examiner does not teach a single instruction memory storing instruction used by a plurality of interface processors. As argued above and incorporated by reference each of the interface processors of Shobatake work from dedicated memory and does not share a common instruction memory as recited in the claim. Sharing instruction from a common instruction memory provides benefits and value in that scarce silicon real estate is conserved to provide other function, whereas independent memory for each processor as taught in the reference depletes the scarce resource, an undesirable outcome.

Similar errors are found in the Examiner's assertion that elements of the separately patentable dependent claims are found in Shobatake et al.

CONCLUSION

Based upon the above arguments claims 10-13, 43 and 44 define patentable subject matter and are not anticipated by the cited prior art. As a consequence the Examiner's final rejection of claims 10-13, 43 and 44 should be reversed.

Respectfully submitted,



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Appendix of Rejected Claims:

10. A method comprising the steps of:

storing in a single instruction memory instructions for the handling of data transiting an interface device;

executing in a plurality of interface processors the instructions stored in the single instruction memory;

receiving a data flow inbound through an input port;

communicating the data flow through the plurality of interface processors; and

directing the data flow outbound through an output port in accordance with the execution of the instructions by the interface processors.

11. A method according to Claim 10 further comprising parsing the data flow into a plurality of portions, storing selected portions of the parsed data flow in data memory, and directing other selected portions of the parsed data flow to a switching fabric for determination of an outbound direction.

12. A method according to Claim 11 further comprising recombining the stored and other selected portions of the data flow prior to direction of the data flow outbound through an output port.

13. A method according to Claim 10 wherein the step of communicating the data flow through the plurality of interface processors comprises parsing the data flow into portions and distributing the parsed portions among the plurality of interface processors for handling in parallel.

43. A method according to claim 10 further comprising storing in a control processor control information including initialization and configuration data; and

forwarding stored information to selected ones of said plurality of interface processors.

44. The method according to claim 43 wherein the control information is forwarded in a packet formatted with a protocol compatible for a network coupling the control processor and the interface processors.